REMARKS

These remarks are in reply to the Office Action mailed October 20, 2005. Claims 1-17 stand rejected under 35 U.S.C. 103(a). Claims 1-2, 5-8, 11-15, and 17 have been amended. New claims 18-20 have been added. Applicant respectively traverses the rejections.

Claim Rejections - 35 U.S.C. 103(a)

Claims 1-3, 6-9, and 12-15 stand rejected under 35 U.S.C. 103(a) as not being patentable over U.S. Pat. to Zhu[1] ("Zhu") and U.S. Pat. to Rinaldi, et al.[2] ("Rinaldi") in view of U.S. Pat. Pub. to Zeidler[3], et al. ("Zeidler").

When hosts communicate with a display device through known graphics controller chips, the controller adds a delay to the communication. The present invention avoids storing and processing data in the graphics controller chip. It also avoids the necessity to synchronize the movement of data through the graphics controller chip. Amended claim 1 is directed to graphics controller *chip* for providing an interface between a graphics display device and a host, and for permitting the host to communicate directly with the graphics display device. Amended independent claims 6 and 13 are similar.

The graphics controller chip of amended claim 1 includes:

> "an output bus for coupling to the graphics display device;" and
>
> "an on-chip video processing circuit having . . . an output coupled to the output bus of the graphics controller."

According to the Office Action, Zhu teaches a graphics controller by reason of a graphics coprocessor 11 disclosed in the reference, and a video processing circuit having an output bus coupled to a graphics controller by reason of a graphics accelerator 15 included in the graphics coprocessor 11. Zhu does not show an output bus coupled to a

---

[1] No. 5,423,009
[2] No. 6,327,002
[3] No. 2003/0001970

graphic display device. The Office Action maintains, however, that Zhu inherently teaches these items.

Applicant respectfully disagrees with the rejection of amended independent claims 1, 6, and 13 for the reason that no aspect of Zhu is disclosed as being disposed in a single chip, and because Zhu fails to disclose an output bus coupled to both a display device and the output of an on-chip video processing circuit.

First, Zhu makes no mention of how the blocks shown in the environment[4] shown in Figure 1 are implemented. The amended claims clarify that graphics controller of the present invention is a single chip. As Zhu makes no mention of how the blocks are implemented, the reference does not disclose a chip having disposed therein a video processing circuit and an output bus coupled to the output of the video processing circuit and to a display device.

Second, while an output bus may be inherent somewhere in the Zhu environment, Zhu does not disclose *where* the output bus would be coupled to the Zhu environment. In contrast, the output bus of the present invention is coupled to specific locations, namely to the output of the video processing circuit and to a graphics display device. One of ordinary skill in the art would likely understand that if an output bus and a display device are inherent in the Zhu environment, then Zhu suggests that this output bus would be coupled to the shown *VGA controller 13*[5] and not, as the Office Action suggests, to the graphics accelerator 15 (also referred to as a window accelerator).[6] One reason is that it is well known that VGA (Video Graphics Array) is a computer *display* standard originally implemented in a single (gate-array) chip, and a controller is a device designed to convert image data typically stored in a memory (such as display memory 19) into a signal for input to a display device. Another reason is that one of ordinary skill would likely recognize that an accelerator is a device for speeding up certain operations, and which does not have an inherent capability to drive a display device using the protocol

---

[4] Zhu, Col. 2, lines 39-40.

[5] See, for example, Figure 1, Intel Application Note 735, which shows a VGA controller coupled to a 386 processor and a VGA monitor. Zhu refers to Intel 386 processors in Col. 1, lines 24-27 and 63-64. The Fujimoto reference (Pat. No. 5,479,183) cited in the Office Action provides another example: "The graphic subsystem 51 is a Video Graphic Array (VGA) adapter used for controlling a selected display, based on image data stored in the VRAM 27." Col. 4, line 67, Col. 5, lines 1-2.

[6] Zhu, Col. 2, lines 58-59.

required by the device. Thus, while Zhu discloses a bus between the output of the window accelerator 15 and the memory controller 21, the reference does not disclose that this bus is an output bus coupled to both a display device and the output of an on-chip video processing circuit.

According to the Office Action of October 20, 2005, Zhu is said to disclose a bypass path adapted to switchably couple the input bus of the graphics controller to the output bus of the graphics controller. Applicant respectfully disagrees as Zhu fails to disclose a bypass switching circuit. Zhu merely discloses a bus connection, and does not disclose a bypass switching circuit adapted for switchable coupling. As this was explained in Applicant's amendment filed August 15, 2005, this argument is not repeated here.

As mentioned, Zhu does not show an output bus coupled to a graphic display device. The Rinaldi reference, however, shows a display 14 connected to a graphics controller 24. According to the Office Action, it would have been obvious to one of ordinary skill in the art to combine the teachings of Rinaldi into the system of Zhu. Specifically, the Office Action would import the Rinaldi display 14 and its connection to the graphics controller 24 into the Zhu system to supply the missing output bus and display device. In other words, the Office Action argues that it would be obvious to connect the Rinaldi display 14 to the Zhu graphics accelerator 15. For the reasons stated below, Applicant respectfully disagrees.

First, the Rinaldi reference discloses that a video graphics controller may be bypassed using components disposed on the video graphics card 12 other than those within a graphics controller chip. Thus, the Rinaldi reference *teaches away* from providing a bypass of a video processing circuit within a chip. "It is improper to combine references where the references teach away from their combination."[7] Accordingly, Rinaldi may not be combined with Zhu for the purpose of providing a suggestion to supply the output bus and display device missing from Zhu.

In addition, the present invention is directed to a graphics controller chip, but the Rinaldi reference is directed to a *video graphics card* 12 that includes a graphics

[7] MPEP 2145, X. D. 2.

controller 24. The Rinaldi reference reveals nothing about the internal features of the graphics controller 24. Therefore, Rinaldi fails to suggest a graphics controller chip that includes an output bus coupled to both a display device and the output of an on-chip video processing circuit.

Moreover, neither Rinaldi or Zhu disclose or suggest that one of ordinary skill in the art would couple the Rinaldi display 14 to the Zhu graphics accelerator 15. As described above, the output of Zhu graphics accelerator 15 is not inherently adapted to be coupled to a display device. If one of ordinary skill in the art was inclined, for some reason, to combine the Rinaldi display into the Zhu environment, he would not be likely to connect the display to the bus connecting the window accelerator 15 with the memory controller 21. Instead, one of ordinary skill would be likely to connect the Rinaldi display to the shown VGA controller 13.

According to the Office Action, it would have been obvious to one of ordinary skill to combine a graphics bypass switch disclosed in the Zeidler reference with the Zhu system as combined with the Rinaldi display. The graphics controller chip of amended claim 1 also includes:

"a bypass switching circuit *in the chip* . . . "

Applicant respectfully disagrees as Zeidler fails to disclose a bypass switching circuit *in a chip.*

The Zeidler reference is directed to a set-top terminal 10 coupled to a cable input from a CATV network. The set-top terminal system includes a OSD (on-screen display) graphics subsystem 40, a graphics bypass switch 24, and a bypass path 22. Figure 1 shows that the bypass switch 24 and the bypass path 22 are outside of the OSD subsystem 40. The Zeidler graphic subsystem 40 includes an OSD insertion unit 44 and a D/A converter 46, which "may comprise a single chip or chip set."[8] Plainly, Zeidler fails to disclose that either the graphics bypass switch 24 or the bypass path 22 are disposed in a graphics controller chip.

[8] Zeidler, paragraph [0014]

In addition, the Zeidler publication, like Rinaldi, *teaches away* from the claimed invention. Because Zeidler discloses an off-chip graphics bypass switch and an off-chip bypass path, the reference teaches away from providing these features in a chip. As mentioned, it is improper to combine references where the references teach away from their combination. Accordingly, it is improper to combine Zeidler with other references in order to show the obviousness of the claimed invention.

Claims 2-5, and 12 depend from independent claim 1 and are patentable for the same reasons expressed above that claim 1 is patentable. In addition, claims 7-11, and 18-20 depend from claim 6 and are patentable for the same reasons expressed above that claim 6 is patentable. Further, claims 14-17 depend from claim 13 and are patentable for the same reasons expressed above that claim 13 is patentable.

Claims 4-5, 10-11, and 16-17 stand rejected under 35 U.S.C. 103(a) as not being patentable over U.S. Pat. to Zhu[9] ("Zhu") and U.S. Pat. to Rinaldi, et al.[10] ("Rinaldi") as applied to claims 1, 3, 6, 9, and 13, and further in view of U.S. Pat. to Fujimoto[11] and U.S. Pat. to Clark.[12]

According to the Office Action, Clark discloses a plurality of LCD panels and Fujimoto discloses a display controller for selecting one of a plurality of display panels. The Office Action maintains that it would have been obvious to one of ordinary skill in the art to combine the plurality of displays taught by Clark and Fujimoto into the single display system of Zhu and Rinaldi. Claim 4 comprises the claimed graphics display device that further comprises:

> "a plurality of LCD panels, and wherein the graphics controller includes a panel select switch for selecting *one* of the panels to receive data from the output bus of the graphics controller.

Claims 10 and 16 are similar. Applicant respectfully disagrees as it would not have been obvious to one of ordinary skill in the art to combine the plurality of displays taught by Clark and Fujimoto with the other cited references.

---

[9] No. 5,423,009
[10] No. 6,327,002
[11] No. 5,479,183
[12] No. 5,949,437

The Fujimoto reference discloses a display detecting apparatus for a computer system. The display detecting apparatus "can check . . . to see if an optional display is connected when the power supply is started in a resume mode."[13] A display controller (DISP-CONT) 24 drives a selected one of the LCD 37 and CRT display 49.[14] Fujimoto Figure 6 shows that if an optional CRT is connected to the system during VGA initialization, the optional CRT is automatically selected. Fujimoto does not teach or suggest a panel select switch for selecting by a host of one of a plurality of display devices connected to a graphics controller chip.

The Clark reference discloses a "a circuit board environment for driving multiple displays of the same type."[15] According to Clark, multiple monitors may be desired in a variety of contexts, such as where one display faces the customer on the outside and one display faces the operator on the inside.[16] Clark discloses a single frame buffer 18 and graphics circuitry 16 that provides two outputs: a first video output for use by a first display 20 and a second video output for use by a second display 22.[17] Thus, the Clark reference discloses simultaneously driving two displays with the same data.

In contrast to Clark where two displays are simultaneously driven, the panel select switch of the present invention selects only one of a plurality of display devices. "If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or modification to make the proposed modification."[18] Therefore, Clark may not be relied on to support the rejection for the reason that Clark would only be able to drive a single one of the plural displays following the proposed modification.

Therefore, claims 4, 10, and 16 are not obvious under 35 U.S.C 103(a) over Zhu and Rinaldi in view of Clark and Fujimoto because there is no motivation to combine Clark with the other references cited and Fujimoto fails to disclose a panel select switch.

---

[13] Fujimoto, Column 2, lines 35-40.
[14] Fujimoto, Column 4, lines 37-40.
[15] Clark, Col. 2, lines 1-4.
[16] Clark, Col. 2, lines 24-29.
[17] Clark, Col. 2, lines 42-50.
[18] MPEP 2143.01 V.

Claim 5 depends from claim 4, claim 11 depends from claim 10, and claim 17 depends from claim 16. Claims 5, 11, and 17 are therefore patentable for the same reasons expressed above that claims 4, 10, and 16 are patentable.

Conclusion

Accordingly, claims 1-20 are in condition for allowance. Applicant requests that claims 1-20 be allowed, and this application be passed to issue.

Respectfully submitted,

Richard A. Wilhelm
Reg. 48,786
Of Attorneys for Applicant